

FIG. 1

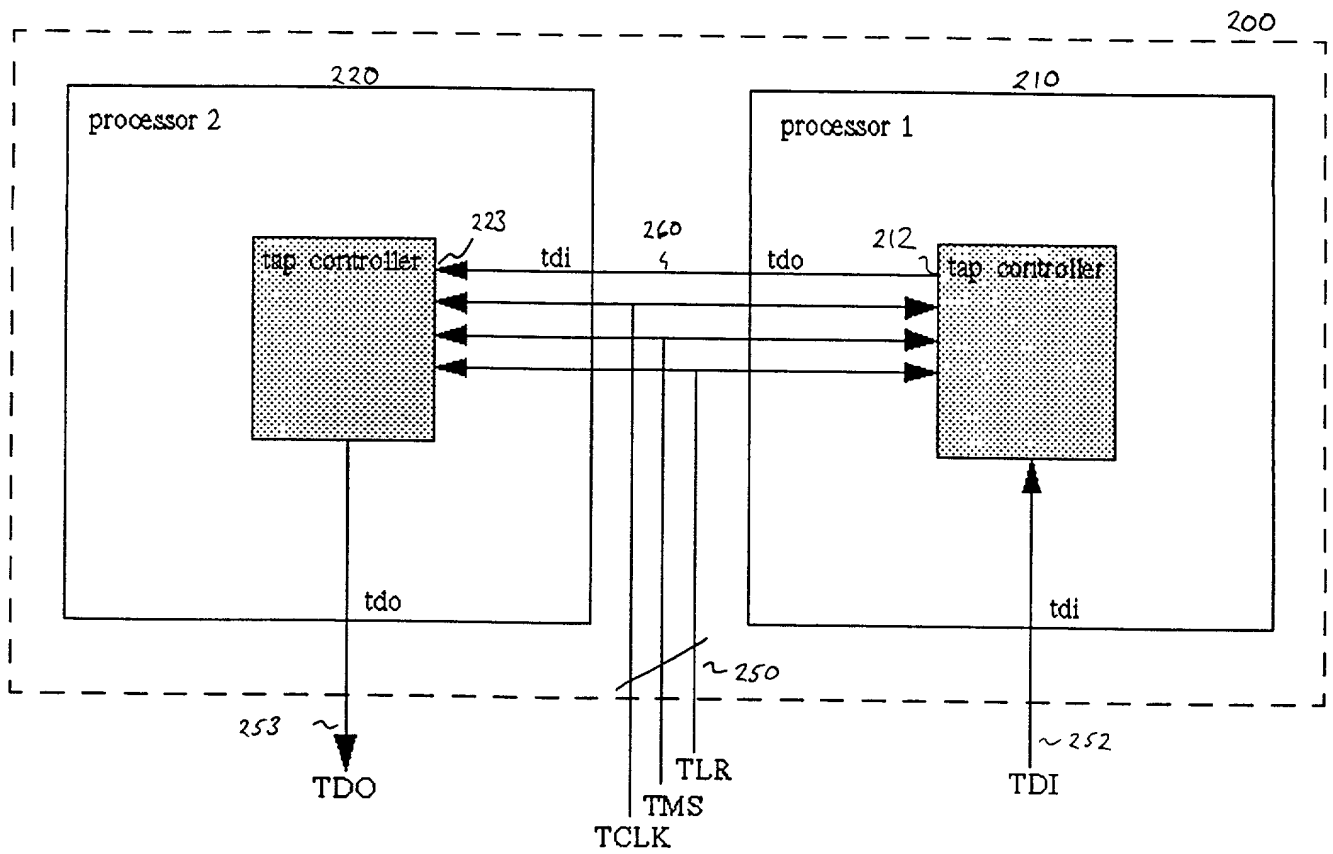


FIG. 2

Fig 3a

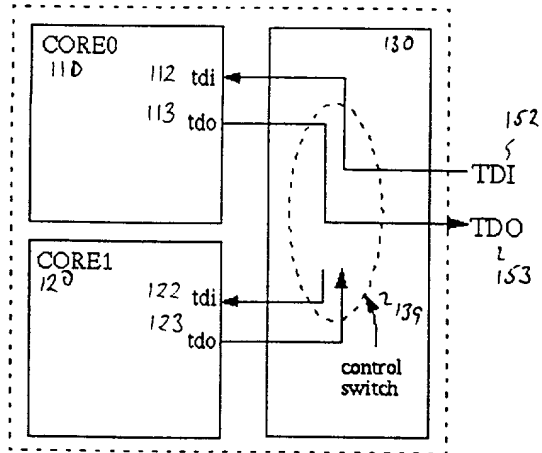


Fig 3b

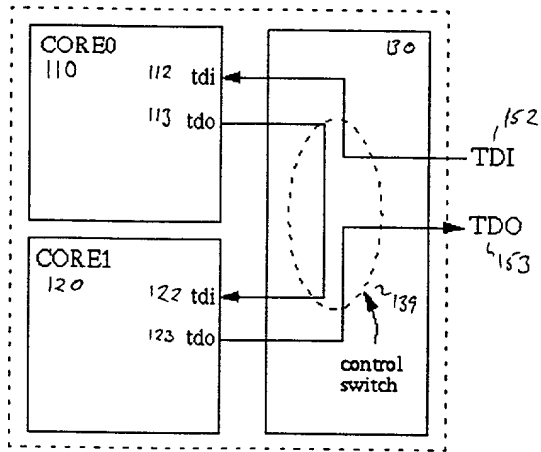
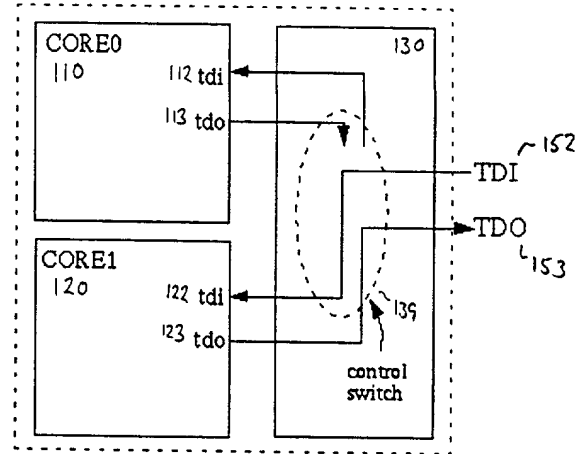


Fig 3c

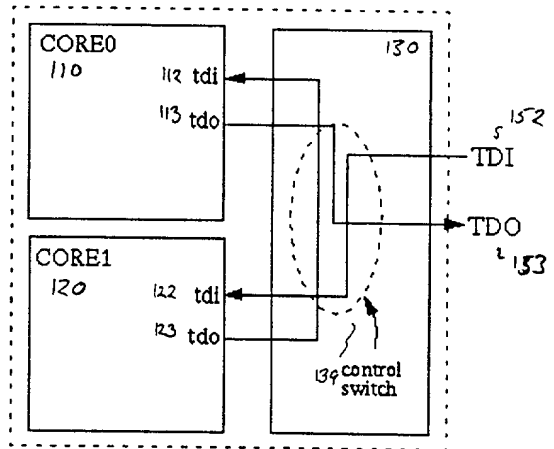


Fig 3d

Fig. 4a

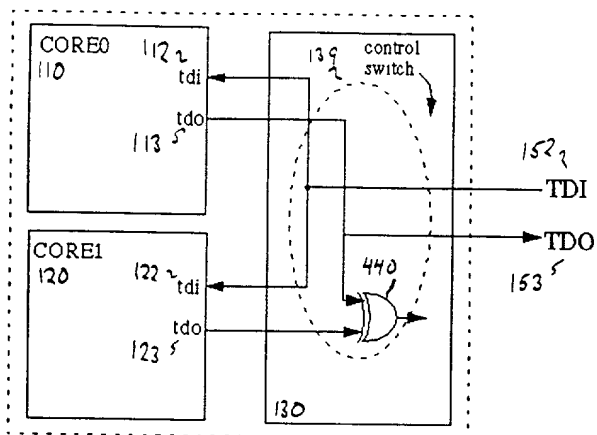


Fig 4b

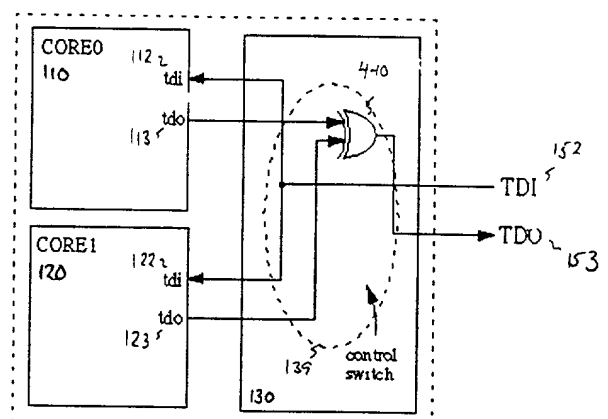
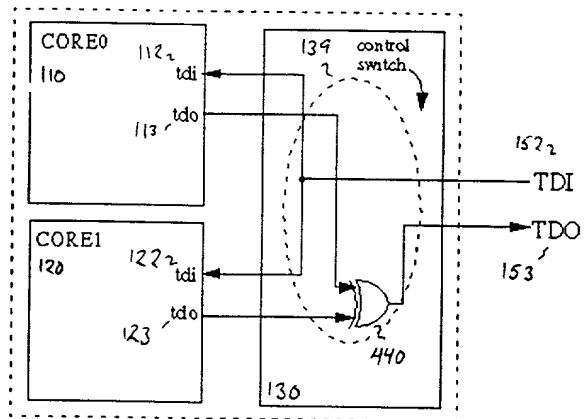
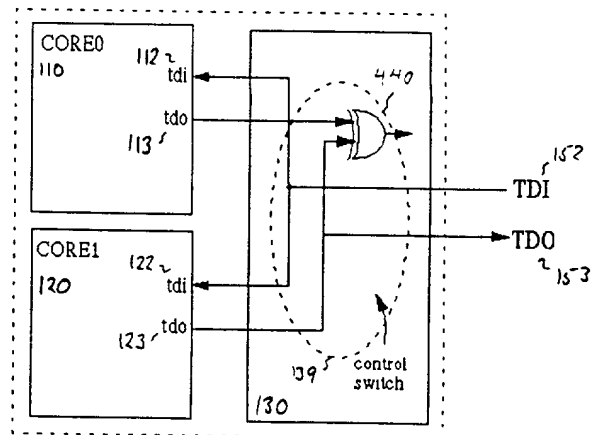


Fig 4c

Fig 4d

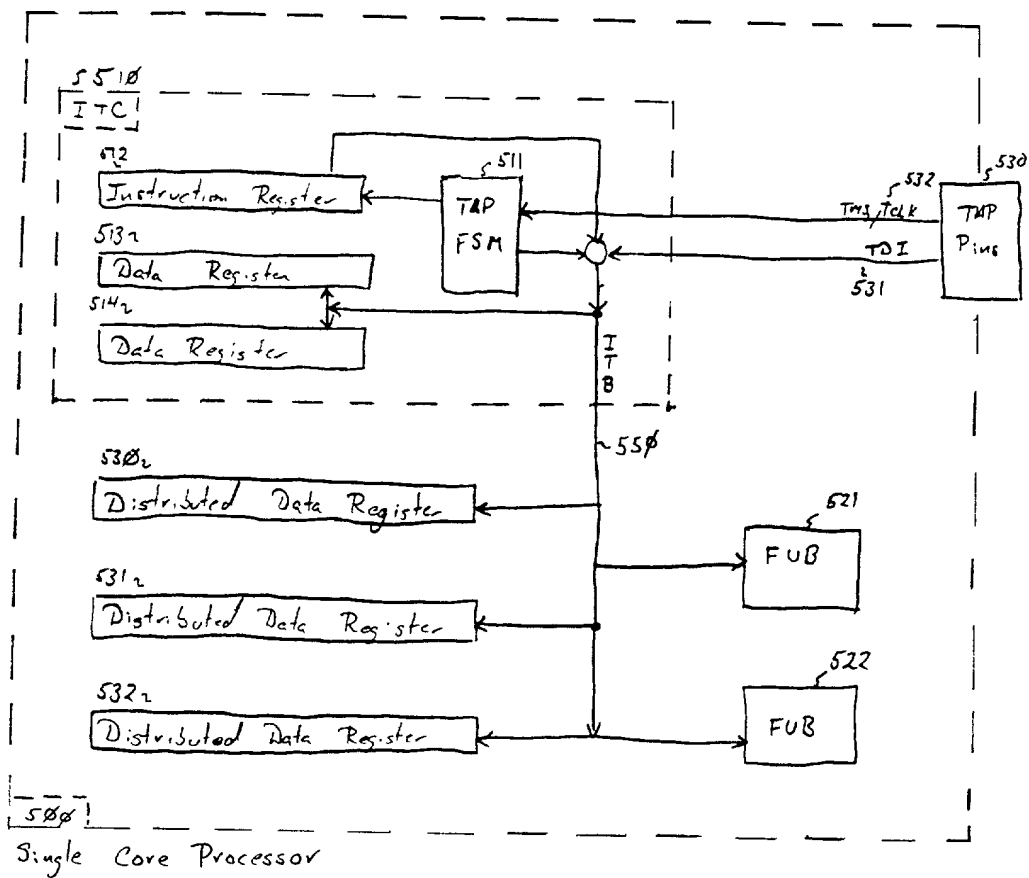
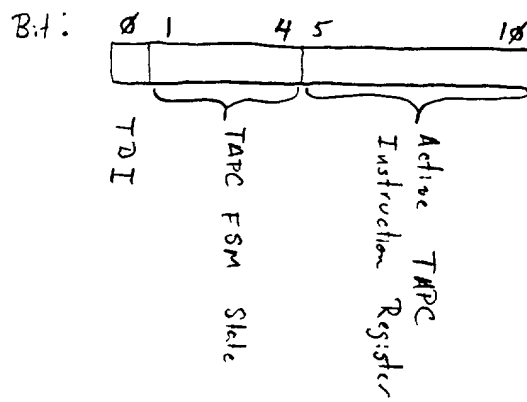


Fig. 5

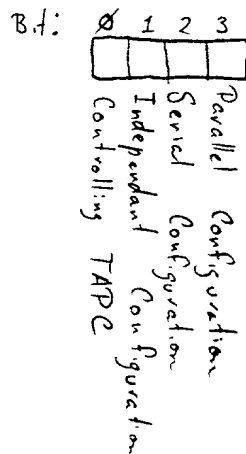
Fig. 6



Integrated Test Bus

Fig. 7

TAP Core Configuration Register



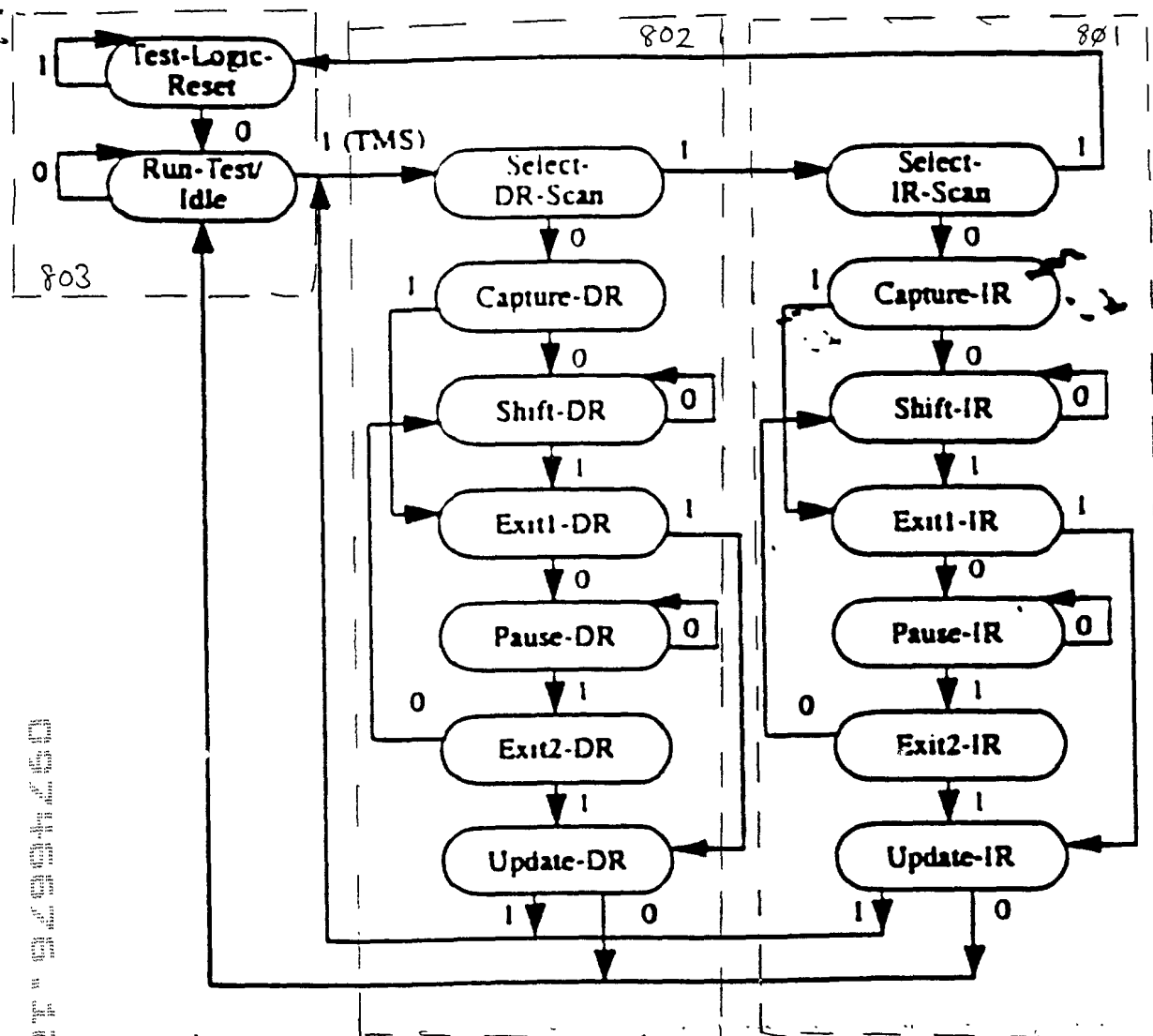


Fig. 8

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